A High-Performance AGC System for Home-Brew Transceivers

Ham-band conditions create a severe strain on any receiver. This AGC system provides smooth gain control with no ear-splitting pops and clicks.

By Mark Mandelkern, KN5S

Amid the glowing reviews and happy reports of the newest developments in receiver technology, one still sometimes finds complaints of AGC troubles—pops, clicks, and other characteristics of poor AGC performance. A ham shack is an environment totally different from a lab test bench or a commercial station. A receiver that functions beautifully when connected to a signal generator, or even several generators at constant level, or when tuned to a single station, may be completely unusable with a ham antenna attached. For real-world amateur operation we need immediate, silent, automatic adaptation to dynamic signals of vastly different levels.

A good AGC system should react instantly, with no popping noise, to signals suddenly appearing at a level 100 dB over the residual noise in a quiet receiver. One should not hear receiver rushing noise between CW dits or SSB syllables. When a strong signal disappears, the receiver should be almost instantly ready to hear a weak signal right down at the noise level.

Although it took three years to design and build, most portions of my home-brew transceiver (Fig 1) caused no special trouble. But obtaining the desired AGC performance required more elaborate measures than expected and even a special AGC test device. The results were well worth the effort; the resulting AGC system performs beautifully, and the home-brew transceiver has been in constant use for the last three years. The AGC system and the special test device will be described here.

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Fast or Slow?

It can be quite misleading to label an AGC mode as simply fast, medium or slow. In fact, there are three timing periods involved: attack time, hang time and recovery time. These are sketched in Fig 2. While the mode designation should refer to the hang time, most receivers unfortunately have no hang circuit, and the designation thus refers to the recovery time.

The attack time is perhaps the most crucial; trouble here is often responsible for clicks and pops on the leading edge of a strong CW or SSB signal. Filter delay and incorrect attack time can also result in overshoot, where the leading edge of a dit causes a pop, because of AGC lag, followed by overcorrection and excessive receiver gain reduction. Just what you're listening for—perhaps a DX signal report—is made to sound weaker! The fast, medium and slow designations do

not apply to this first timing period. A receiver should be designed for immediate adaptation to any signal level. Unfortunately, some receivers employ an excessive recovery time to compensate for inadequate attack performance. This leaves the pop on the first dit but reduces the receiver gain during the rest of the transmission so that more pops are not heard. The great disadvantage of this band-aid method is slow recovery. When the strong locals stop calling, the receiver is not ready for the weak DX station for maybe one or two seconds. Too late to hear him come back to you! A common practice for circumventing this problem is to turn the AGC off; hearing damage can result! The proper attack time for a given receiver depends on the selectivity, the nature of the filters and the resultant filter delay.

The hang portion of a proper AGC system is not always included in modern receivers. It is simpler to include a slow recovery—just a capacitor—but the results are quite undesirable, as explained above. A slow recovery involves a simple R-C circuit with a gradual decay in AGC voltage, perhaps several seconds being required for full receiver gain recovery and reception of the weakest DX signals. On the other hand, a proper hang circuit maintains a nearly constant AGC voltage between dits or syllables, then cuts out completely, allowing the recovery circuit to quickly bring the receiver up to full gain. It is the hang circuit that should be adjustable because of the differences between competitive and casual operation. For fast, medium and slow, I use hang times of 100 ms, 300 ms and 3 s. Some operators choose different AGC timings for CW and SSB; however, this usually means that recovery time is being used to compensate for other AGC deficiencies. With the system described here, performance on CW and SSB is the same, as it should be. I almost always use medium; sometimes slow for ragchewing, and occasionally fast for unusual noise or QRM conditions. The AGC is turned off only for tests and measurements.

The last timing period, the recovery, is very simple, provided it is not improperly used to compensate for the lack of a hang circuit, or for inadequate attack performance. When the strong signal is gone, and the hang circuit has held for as long as you've asked it to, you want full recovery as quickly as possible. A 100-ms recovery does this smoothly.

Filter Delay

The IF strip in this receiver uses very sharp CW and SSB filters, both at the input *and near the output*. No AGC is applied to the receiver front end before the first filter for optimum weak-signal performance. The AGC detector senses signal level after the second filter; otherwise it would sense signals that you don't hear and cause an unwarranted decrease in gain for the weak signal you want. In order to prevent a pop on the leading edge of a CW dit or an SSB syllable, the system must employ a very fast attack time. But there is a considerable delay through the second filter. This means that the signal at the IF output builds up to a high level before the AGC has a chance to decrease the IF gain; this produces the pop. Even worse, this large signal then appears at the AGC

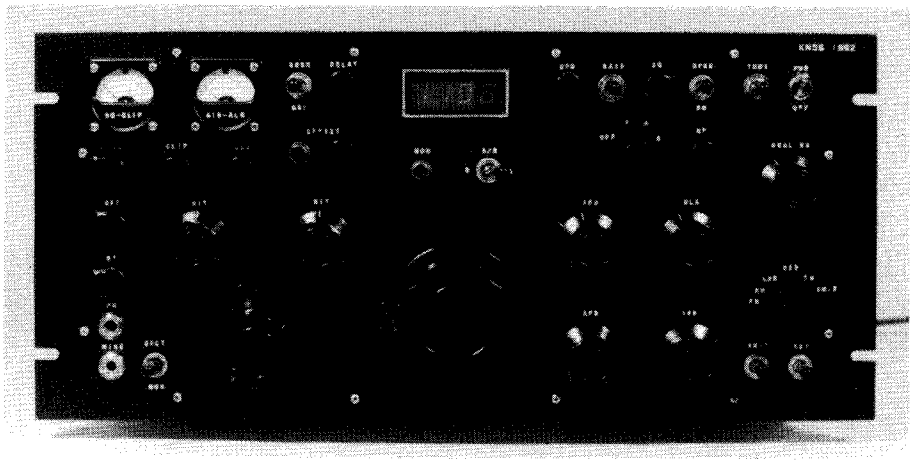


Fig 1—In my home-brew transceiver shown here, the AGC switch is labeled OFF-F-M-S. The SQUELCH (down) switch is part of the OPERATE (up) and STANDBY (center) switch, which is labeled merely OPER-SQ. The meters read signal level in dB and squelch integrator charge. Not shown here are the three separate transceiver front-end sections for MF/HF, 6 meters, and 2 meters.

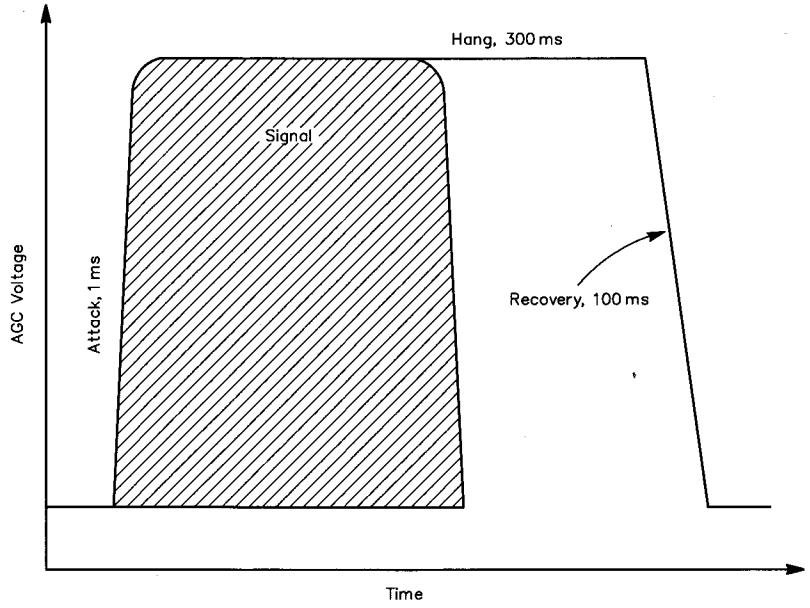


Fig 2—The three AGC timing periods—attack, hang and recovery—shown here in concept, but not to scale.

detector, producing excessive AGC voltage and decreasing the receiver gain, often causing a noticeable dip in AF output; this is the overshoot. The combination of delay and overshoot can even result in AGC oscillations producing distortion in the receiver audio output. Some of these AGC malfunctions are sketched in Fig 3.

Dual-Attack Timing

This, then, is the problem. Filter delay makes it impossible for any simple AGC system to maintain instantaneous gain control. The result is either popping, or overshoot, or both. R. L. Drake's solution was a dual system (see acknowledgments at the end of the article). The circuitry is surprisingly simple. The IF strip is separated into two parts, called IF1 and IF2. The output filter is moved to a position between them where it performs its function just as effectively. The two portions of the IF strip are then provided AGC voltages with different characteristics.

A block diagram of the IF system is shown in Fig 4. The first portion, IF1, consisting of the amps before the second filter, receives a delayed AGC voltage, denoted AGC1. The time constant is chosen, using the special test device described below, to eliminate overshoot and obtain smooth control of IF1. Now this leaves a pop at the input of IF2, but it doesn't reach the headphones because an undelayed AGC voltage, denoted AGC2, controls IF2 almost perfectly. The AGC detector is at the end of IF2, so there is no filter in the IF2-AGC2 loop. In my home-brew transceiver, the 9-MHz IF strip consists of six MOSFET amps, split four and two into IF1 and IF2. The action of AGC1 on IF1 is sluggish, but smooth, in its response to signals at different levels, while IF2 reacts almost instantaneously to AGC2. During the leading edge of an initial dit or syllable, only AGC2 at IF2 functions, maintaining constant receiver output level while giving IF1 a chance to catch up. On this leading edge, the AGC2 voltage applied to IF2 may be very high, but it's all too quick even to be seen on the S-meter. As the AGC1 voltage to IF1 rises gradually (meaning over several milliseconds), the AGC2 voltage drops. During this process the overall IF gain is constant, but shifts from being derived mostly from IF1 to a balanced state.

An additional valuable feature of this system is that AGC2 reduces a short static pulse to the receiver operating level, even more effectively than noise-clipping.

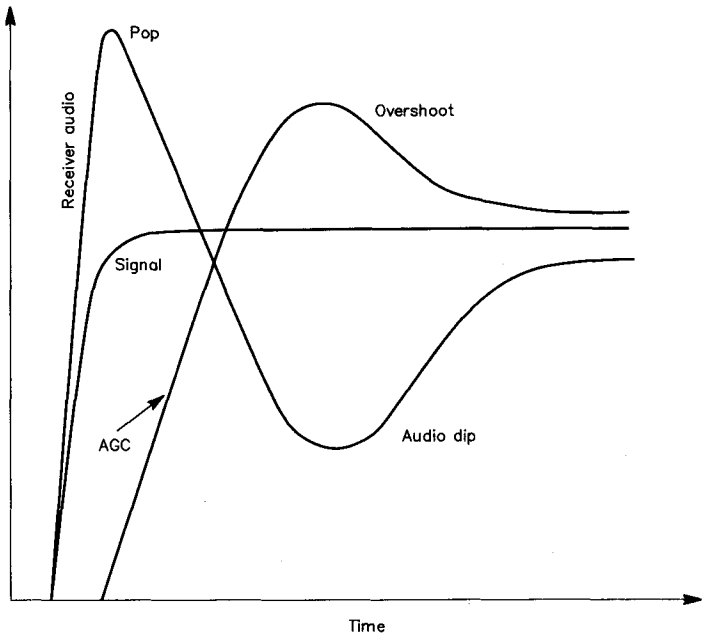


Fig 3—AGC problems to be avoided—slow attack time and AGC overshoot. This rough sketch is not to scale.

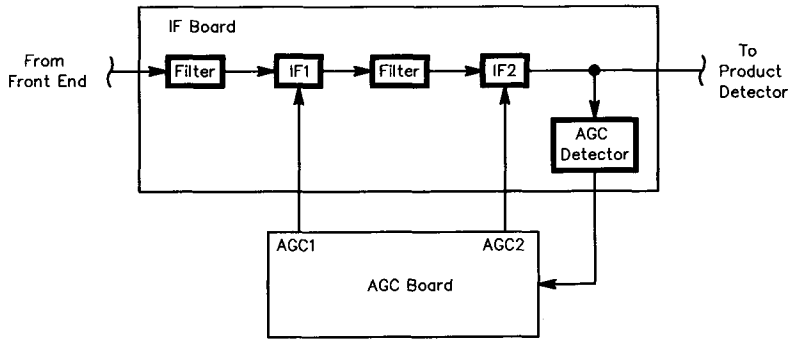


Fig 4—Block diagram of the IF system.

Circuit

A block diagram of the AGC system is shown in Fig 5. A general description of the system will be given here. The block diagram shows all the active circuit elements and certain other important components mentioned in this general description using a symbolic pseudo-schematic abbreviated representation. The five sections will be discussed in detail under separate headings; complete schematics are shown in Figs 6-9 and 11.

The detector section includes an AGC amplifier, which ensures that

Fig 5 (right)—Block diagram of the AGC system. This shows the active circuit elements and certain other important components using a symbolic pseudo-schematic abbreviated representation. Circles are transistors, triangles are op amps. For the actual circuits, the schematics in Figs 6-9 and 11 must be used. Potentiometers labeled in CAPITALS are front panel controls; those labeled in lower case are trimpot adjustments on the circuit board inside the radio.

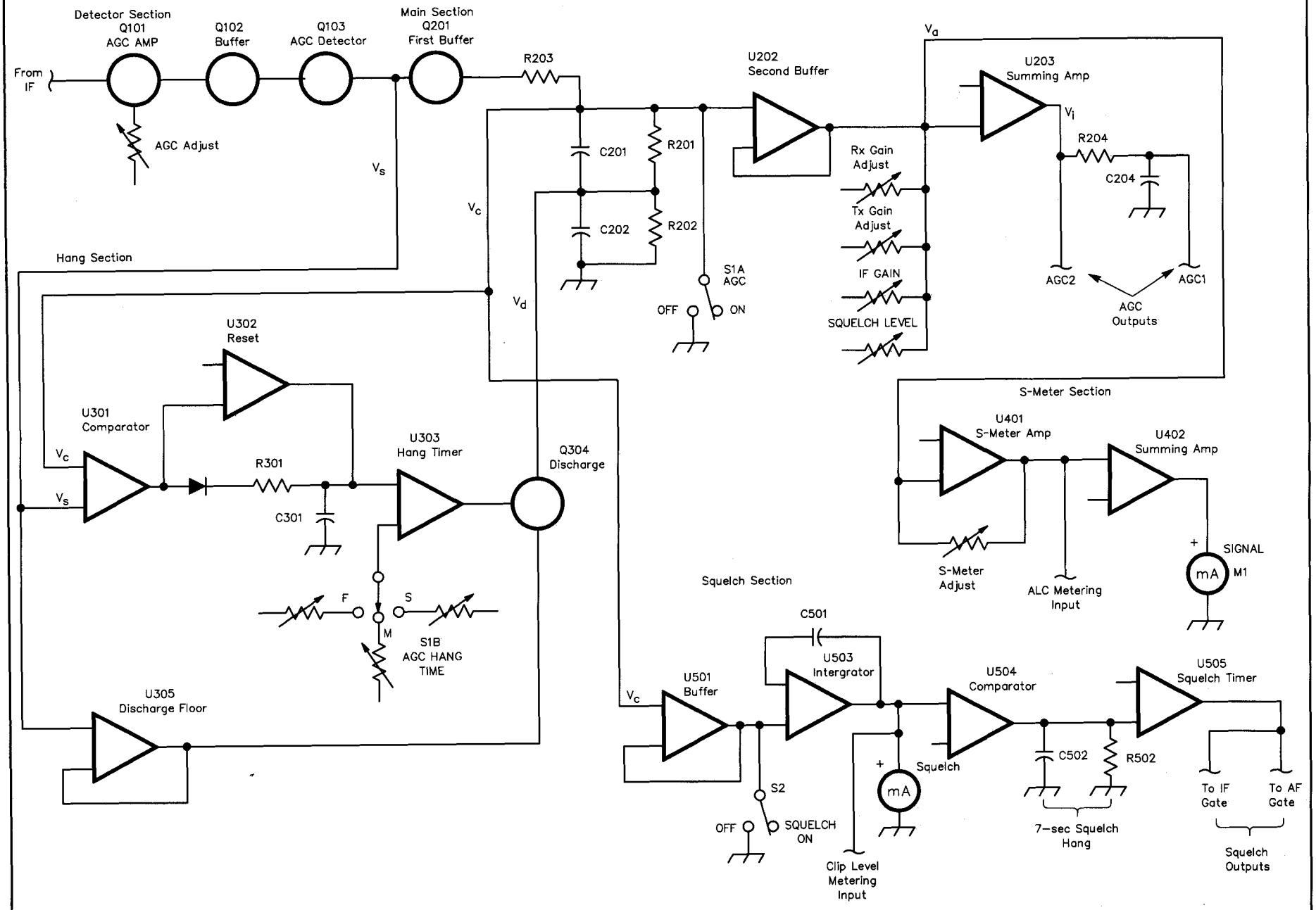
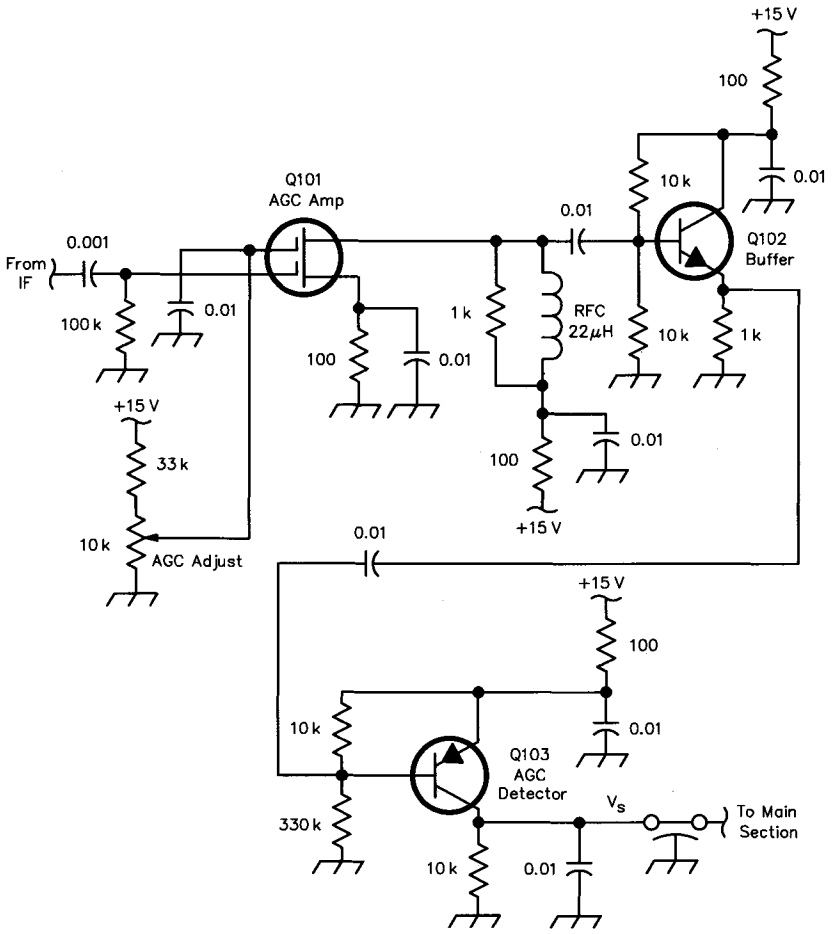

Detector Section
Q101
AGC AMP
Q102
Buffer
Q103
AGC Detector
Main Section
Q201
First Buffer
From IF
AGC Adjust
V_s
R203
C201
R201
C202
R202
V_c
V_d
U202
Second Buffer
V_a
U203
Summing Amp
V_i
R204
C204
Rx Gain Adjust
Tx Gain Adjust
IF GAIN
SQUELCH LEVEL
AGC2
AGC1
AGC Outputs
S1A
AGC
OFF
ON
Hang Section
U302
Reset
U301
Comparator
V_c
V_s
R301
C301
U303
Hang Timer
Q304
Discharge
F
S
M
S1B
AGC HANG TIME
U305
Discharge Floor
S-Meter Section
U401
S-Meter Amp
U402
Summing Amp
S-Meter Adjust
ALC Metering Input
+
mA
SIGNAL
M1
Squelch Section
C501
U503
Intergrator
U501
Buffer
V_c
U504
Comparator
U505
Squelch Timer
+
mA
Squelch
C502
R502
S2
OFF
SQUELCH ON
Clip Level Metering Input
7-sec Squelch Hang
To IF Gate
To AF Gate
Squelch Outputs

Fig 6—Detector section schematic diagram. This section is located on the IF board, while the remainder of the AGC system is on the AGC board. Each board in the transceiver is mounted in a separate copper box; the feed-through capacitors, 0.001 μF, indicate where leads leave the box. In addition to the feed-throughs, each lead is filtered outside each box, using a π-section filter consisting of a 1-mH RFC and two 0.1-μF monolithic ceramic bypass capacitors. Almost all components are available from Digi-Key Corp, Box 677, Thief River Falls, MN 56701-0677, tel: 800-344-4539, 218-681-6674; fax: 218-681-3880. All resistors are 1/4-W, 5% carbon-film types. The diodes are small-signal types, such as 1N4148. The 1-μF capacitors are monolithic ceramic types; those of higher capacity are 20-V electrolytics, tantalum if 10 μF or less. The bipolar transistors may be any small-signal types, such as the 2N4400 (NPN) and 2N4402 (PNP). The MOSFETs used here are type 3N140, but any small-signal RF-type dual-gate MOSFET may be used; they all have roughly the same characteristics at IF frequencies.

Since these circuits are intended for incorporation into other transceiver designs rather than for exact duplication, pin-outs and package arrangements are not given. The op amps are of two types, the regular LM324 op amp and the open-collector comparator LM339. In this circuit all these have the upper supply connection from the +15-V rail, and the LM339 types all have ground as the lower rail. But the LM324 types are used in two different ways; either with the lower supply connection from the −15-V rail or at ground. Although it is conventional to label the supply rails for only one of a package of four op amps, here all rail connections are labeled; this shows the functioning of each device most conveniently. The LM339 types are indicated by a black dot at the output. The stages labeled "comparator" may be either regular op amps used as comparators or actually the open-collector types commonly called "comparators."



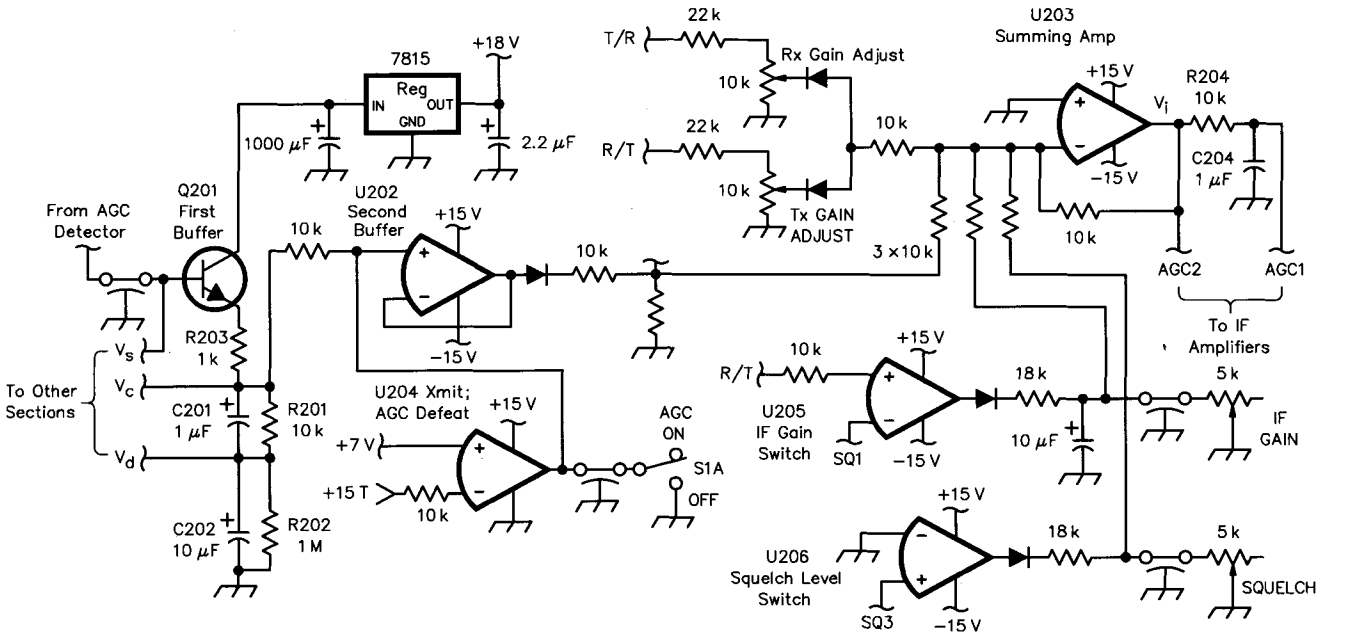


Fig 7—Main section schematic diagram. For schematic conventions used here, see the caption to Fig 6.

there will be AGC voltage available at even the weakest signal levels. The bipolar detector provides the dc signal that is to be processed by the rest of the AGC system.

The main section includes a bipolar buffer for current gain, the main timing capacitors C201 and C202, panel IF GAIN provision, trimpot IF gain adjustment for receive and transmit, panel SQUELCH LEVEL control, and the dual attack timing circuit feeding AGC voltage to the two separate portions of the IF amplifier chain.

The hang section provides three different hang times, set by trimpots and selected by a panel switch. A comparator compares the AGC detector dc level V_s with the level V_c at the main timing capacitors, so that hang timing does not begin until the signal level drops.[1] Further, a voltage follower provides a floor to a bipolar discharge transistor, so discharge proceeds only down to the present signal level.

The S-meter section provides signal level read-out in actual dB. There is no irksome "S-meter zero" adjustment. The S-meter also reads transmitter ALC voltage.

The squelch section is an adaptation of the integrating squelch circuit previously described in *QST*.[2] The previous design, an outboard unit designed for insertion in the speaker line, dealt with receiver audio. Best performance required turning the receiver AGC off and very careful adjustment of the RF and AF gain controls. This was not so bad in itself, and sensing 50-MHz F_2 DX signals less than 1 dB above the noise made this well worth the effort. But switching back and forth to operating mode was rather tedious.

The squelch system used now is built into the transceiver and works off the AGC system. This has facilitated a number of improvements. A panel switch turns on the squelch; this mutes the audio, defeats the IF GAIN control and activates the panel SQUELCH LEVEL control in its place. This latter is set to hold the IF strip just below the AGC threshold. The integrator op amp is biased at just a few millivolts, so any signal that produces a bit of AGC voltage begins to charge the integrator capacitor. When the squelch opens, the AGC is fully functioning. Compared with the older method, with the AGC off, it is easy to imagine what a great advantage this is when a local rock-crusher comes on the calling frequency.

[1]Notes appear on page 22.

Another improvement in the squelch circuit is a fixed 7-second hang. The old method did provide some hang time because the integrator capacitor would charge beyond the threshold, and then slowly decay to the threshold, before the squelch would drop out. But this action depended on the strength and duration of the received signal.

A final improvement is a squelch discharge circuit. While you are fussing with the SQUELCH LEVEL setting, flicking the squelch switch off and on will discharge the integrator capacitor and the squelch hang capacitor imme-

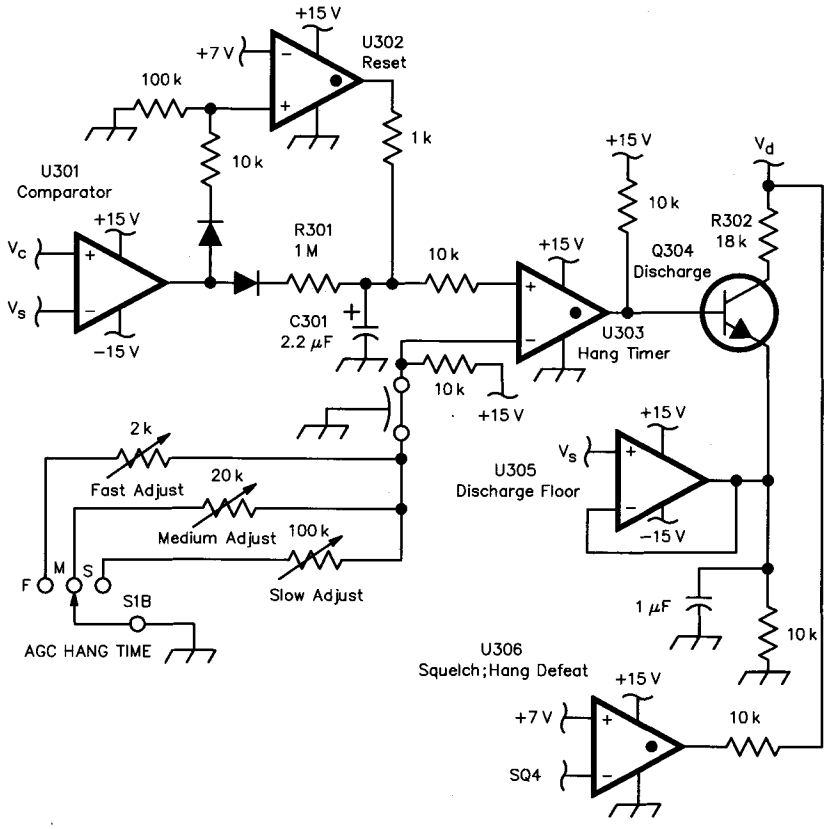


Fig 8—Hang section schematic diagram. For schematic conventions used here, see the caption to Fig 6.

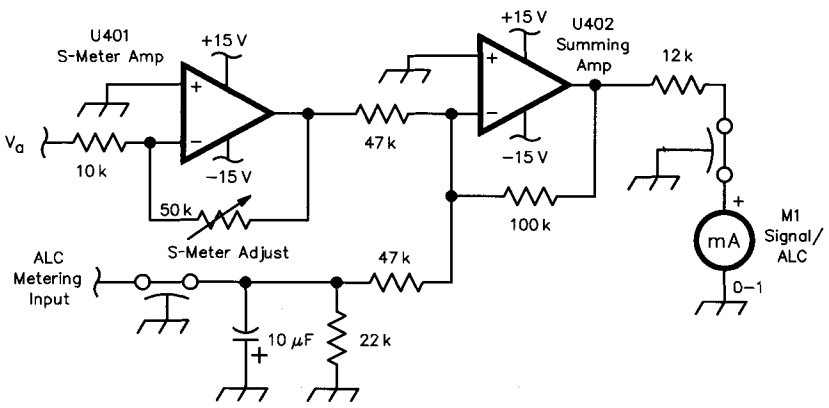
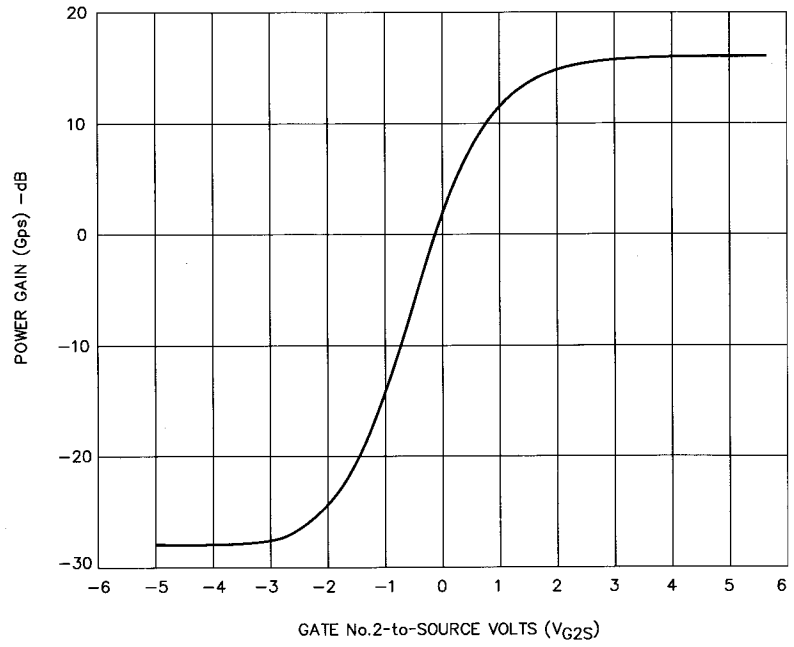


Fig 9—S-meter section schematic diagram. For schematic conventions used here, see the caption to Fig 6.

diately, without waiting 7 seconds.

Detector Section

The schematic of the detector section is shown in Fig 6. Q101 is a simple MOSFET amplifier; the trimpot adjusts the gain of this stage and, in effect, sets the output level of the IF strip. Because of the high gain of the AGC amps, the AGC characteristic is almost perfectly flat, so the question is not "how much AGC voltage do we get?" but simply "what level is required at the input to Q101 to turn on the AGC detector Q103?" The IF output level, at the input to Q101 and at the product detector, is 100 mV P-P (–16 dBm). The Q101 stage receives the IF signal through a buffer that is switched off during transmission. The buffer Q102 is an emitter-follower stage that provides signal current for the AGC detector without excessive loading of the Q101 drain circuit. The PNP detector Q103 is forward biased to V_{be} =0.44 V, just below the conduction point, giving it good sensitivity.



Common-Source Circuit, Gate No.1 Input
Ambient Temperature (T_A) = 25°C
Frequency (f) = 200 MHz
Gate No.1-Votage (V_{G1S})
is Adjusted for I_D = 8 ma
when V_{G2S} = 4 V
Gate No.2 at AC Ground Potential

Fig 10—MOSFET gain versus control gate voltage curve.

Main Section

In the main section, shown in Fig 7, Q201 is another emitter-follower, providing charging current for the timing capacitors C201 and C202. The fast attack and release times, set by R203-C201-R201, are 1 ms and 10 ms, respectively. The hang capacitor C202 charges more slowly. Thus the hang circuit functions only with real signals, not short noise pulses. This prevents AGC hang-up during static conditions. The buffer Q201, with the timing capacitors C201 and C202, form the heart of the system.

The supply voltage for Q201, and thus the charging current for the timing capacitors, is provided by a separate 7815 voltage regulator. In

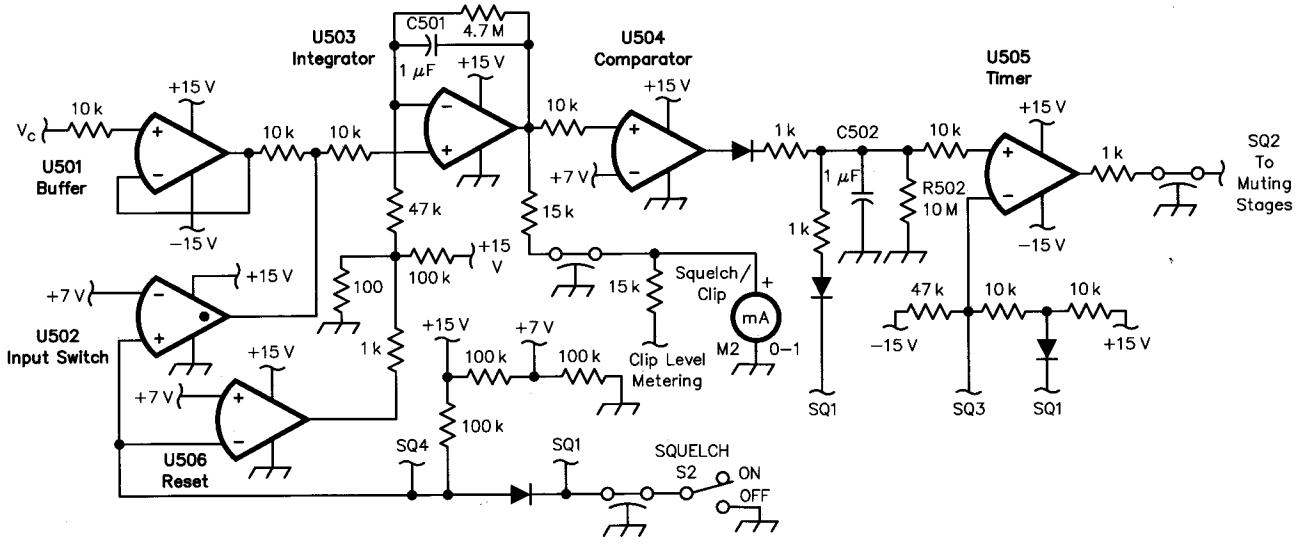


Fig 11—Squelch section schematic diagram. For schematic conventions used here, see the caption to Fig 6.

some receivers, pops, clicks, audio distortion and erratic behavior with signals at the edge of sharp IF filters are caused by transient pulses in the dc supply lines. The circuit that charges the AGC capacitors can cause some of this. The problem is avoided here with the separate regulator and its large filter capacitor. In effect, the initial leading-edge charging current for the timing capacitors comes from this filter capacitor.

To further avoid this and other transient problems in the receiver, the power supply on the rear panel produces regulated +18 and –18-V lines fed to each circuit board. Each board then has on-card regulators for +15 and –15 V. The IF board also has the separate AGC regulator for isolation of Q201, as mentioned. And the power supply also has a separate +18-V supply for the discrete class-AB1 audio output stage, since transients from this stage could otherwise find their way into other circuits. The 5-V supply for the logic circuits and the counter is also separate. These details are mentioned here because providing a pop-free AGC system is not enough; the rest of the radio must also be clean. Transients have even been found to leak between separate power supply circuits run from separate windings on a single transformer. Thus this radio uses four separate small transformers for its four supplies. These comments apply to the basic 39-40 MHz radio shown in Fig 1. The 200-W MF/HF front-end section and the VHF CW/SSB weak-signal front-end sections and driver amplifiers are all separate units.

In this section we identify and designate three distinct system lines. The first two carry dc signals that are sent to other parts of the AGC system. The V_s line carries the voltage developed at the AGC detector and thus represents the actual *signal* level in the IF system. The V_c line carries the voltage at the timing capacitors; it differs from V_s because of the drop in Q201 and the action of the capacitors. The discharge line V_d is used to discharge the hang capacitor C202 at the end of the hang period.

Op amp U202 is a voltage-follower buffer that isolates the timing capacitors, so they are not loaded by the rest of the circuit. The voltage V_c is reduced here to a level we'll call V_a, which is fed to the rest of the AGC system.

The next buffer, U203, the last in the main path of this section, is of a very useful type—an inverting summing amplifier. The key features of this type of amplifier are the grounded noninverting input and the inverse feedback. This results in what is called

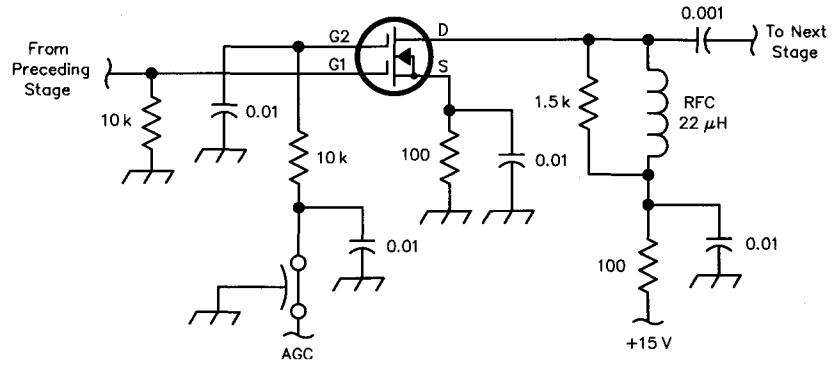


Fig 12—MOSFET IF amplifier schematic diagram of a typical 9-MHz stage. The MOSFETs used here are type 3N140, but any small-signal RF-type dual-gate MOSFET may be used. Each stage in the IF strip is built into its own shielded copper compartment.

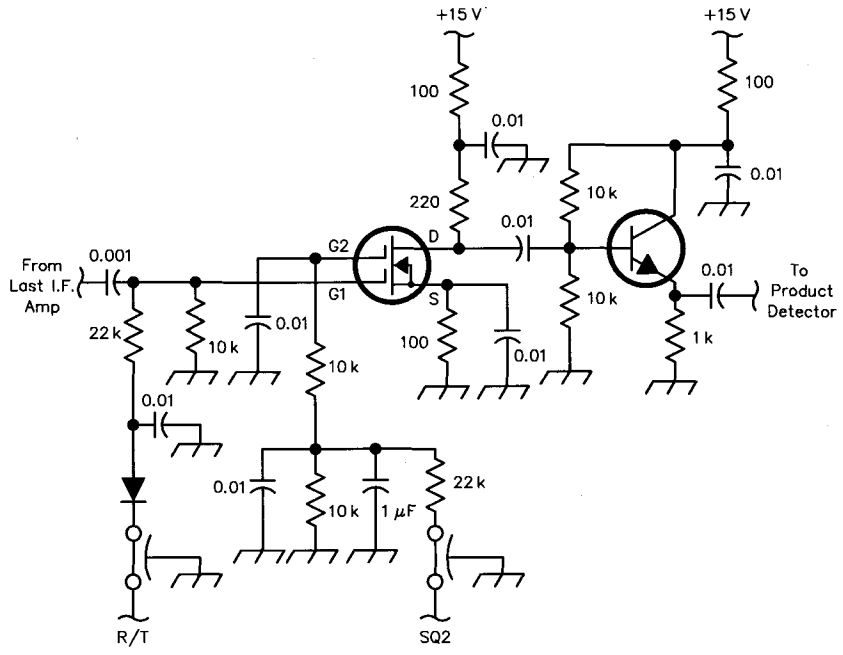


Fig 13—MOSFET IF squelch gate schematic diagram.

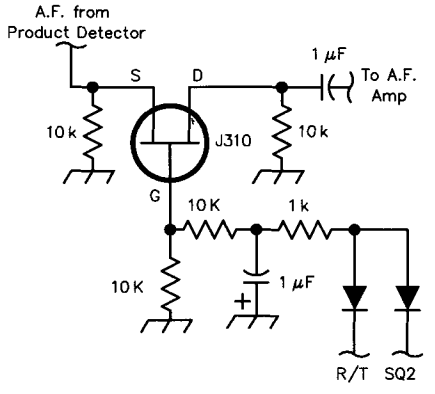


Fig 14—JFET AF squelch gate schematic diagram.

a *virtual ground* at the inverting input. There are five separate inputs to this buffer circuit, but because of the virtual ground, none of these inputs affects the others. Here the stage gain is set at –1, although an inverting summing amplifier may be set up for any negative gain desired. The result is that the op-amp output is the (inverted) sum of all five inputs. Because the IF strip with its crystal filters is also used for SSB transmissions, the T/R and R/T lines (–15/0 V and 0/–15 V in receive and transmit, respectively) are used to switch the receive and transmit IF gain adjustment trimpots.

While transmitting, op amp U204 further disables the AGC system and keeps the timing capacitors discharged, and U205 disables the panel IF GAIN control. During normal receive conditions, the receiver gain trimpot, the panel IF GAIN control and the AGC voltage V_a all sum to produce the control voltage, called V_i, for the IF strip. When the squelch circuit is enabled, the panel IF GAIN control is disabled by U205, and the panel SQUELCH LEVEL control is enabled by U206.

The IF strip uses dual-gate MOSFETs; the AGC lines connect to the gain-control gates. The no-signal AGC line V_i level is nominally +2 V; this is set by the receiver gain trimpot. The AGC voltage V_a from U202 runs nominally from 0 to +4 V, increasing with increasing signal. Since U203 is inverting, V_a subtracts from the +2 V, giving us a +2 to –2-V range for V_i, which will take the MOSFETs from near full gain to near cut-off. These ranges represent the design maximums, for fullest possible gain and fullest AGC control. In my six-stage IF strip the adjustments result in V_i at +1.4 V for no signal and –0.6 V for 120-dB gain reduction. The overall IF strip gain, including filters and pads, is 100 dB.

It is finally at the output of U203 that the dual-attack timing circuit appears. Easily overlooked, though crucial, it consists merely of R204-C204, delaying the AGC1 voltage to the first IF section, IF1. This prevents overshoot, while the nearly instantaneous AGC2 voltage is applied to IF2, keeping pops and clicks from initial dits and syllables out of the headphones.

Hang Section

In the hang circuit, shown in Fig 8, U301 compares the signal level V_s with the capacitor level V_c. Only when the signal drops or disappears, when V_s drops below V_c, does U301 begin to charge the hang timing capacitor C301 to begin the hang period. Note that C301 is merely a timing capacitor controlling the length of the hang period, not the AGC voltage itself; the voltage on C301 increases as the timing period proceeds. Comparator U303 is the hang timer; when the voltage on C301 reaches the level set by one of the fast, medium or slow trimpots, U303 turns on the discharge transistor Q304. Note that the trimpots merely set a dc voltage reference level; they are not actually in the R301-C301 timing circuit. Comparator U302 has a special purpose. Consider the circuit as described so far without U302. Suppose there is a pause in a received transmission, and C301 has already partly charged, say half-way to the set level. A fraction of a second later the transmission resumes and then ends. C301, with no significant load, is still at the half-way point and continues to charge from there. The result is a shortened hang period. U302 corrects this problem. As soon as V_s exceeds V_c, U302 discharges C301, so it is ready to begin the next hang period anew. (The usual way to solve this problem, letting U301 discharge C301 through a diode, will not work easily here. The diode drop is too high in comparison with the low reference level set by the fast trimpot.)

At the end of the hang period, the timer U303 turns on the discharge transistor Q304, which discharges the V_d line through R302. The recovery period is set by C202-R302. The discharge line is not brought to zero, however. After all, only the loudest signal has dropped out; weaker signals may still be in the passband. Dropping the AGC line to 0 at this time could result in AGC pumping (alternating louder receiver output, then over-correction and insufficient output). Voltage follower U305 takes care of this. Without loading the V_s line, it provides a solid floor for discharge transistor Q304, at the V_s level. For example, if an S9 signal disappears and leaves an S5 signal in the passband, after the hang period the AGC line will drop precisely to the S5 level.

S-meter Section

In the S-meter section, shown in Fig 9, U401 senses the AGC voltage V_a from U202 rather than from one of the AGC lines to the IF strip. Thus, the S-meter responds only to signals, and is not affected by the panel IF GAIN or SQUELCH LEVEL controls, or the receive and transmit gain trimpot settings. This method has a great advantage in operating convenience over RF gain controls that push the S-meter up: it

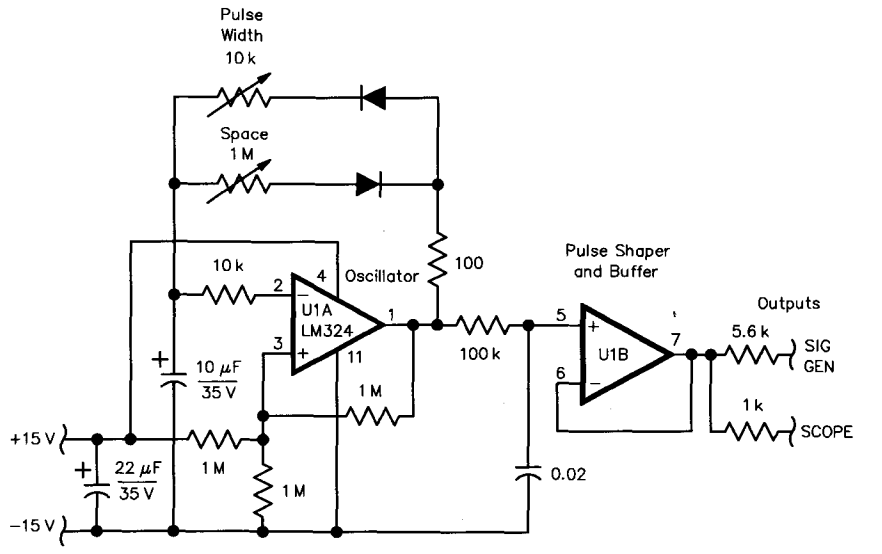


Fig 15—AGC test pulse generator schematic diagram. The 0.02-µF timing capacitor is an accurate, stable type, such as mylar or polypropylene.

allows the S-meter to indicate the signal level relative to the IF gain setting without need for the operator to remember where it was set. It also allows the AGC threshold to be set at the noise level, if desired, with S-meter monitoring of the setting, although there is no need to employ this method. The front-end sections have antenna attenuators and IF output level controls to allow adjustment for optimum gain distribution and dynamic range.

At op amp U401, the trimpot adjusts the gain so the actual 120-dB range of the AGC system produces a voltage of 0 to –6 at the U401 output. The inverting summing amplifier U402 doubles and inverts this, resulting in 0 to +12 V for the S-meter circuit: the 12-kΩ resistor then drives the 1-mA meter M1. With a maximum possible op-amp output of +14 V, this method limits meter overdrive, under any unusual conditions, to 17%.

The MOSFET IF amplifiers are operated in a fairly straight portion of their logarithmic gain curve (see Fig 10). This results in an S-meter that reads very close to actual dB. The MOSFET curve has a very pronounced knee near full gain; if we ran full gain at no signal, S1 might be mid-scale on the S-meter!

The circuit for op amp U402, with virtual ground, causes no interaction between the two input signals: signal level in receive or ALC level in transmit. In transmit the meter reads ALC voltage from the separate front end sections, the station driver amplifiers or the high-power amplifiers. All these are designed to produce –6 V for full-scale meter indication at 20 dB of ALC compression. (In operation about 2 dB is used.) Actual ALC control takes place in the separate front-end sections at signal-frequency stages, but meter read-out is on the main radio panel (Fig 1) for convenience.

Squelch Section

Adapting the original integrating squelch circuit to a squelch system internal to the receiver allowed a great improvement in operating convenience.[2] Here AGC levels are used rather than receiver audio output.

The schematic of the squelch section is shown in Fig 11. Op amp U501 is a voltage follower buffer, which relays V_c to the squelch circuit without loading the timing capacitors. The comparator U502 acts merely as a switch keeping AGC voltage off the integrator when the squelch is off.

The integrator U503, comparator U504 and the metering circuit all function as described in Note 2. The panel SQUELCH LEVEL control, shown in the main AGC section, is set to hold the IF strip gain just below the AGC threshold. When a signal appears, the developed AGC voltage V_c', buffered by U501, causes the integrator capacitor C501 to begin charging. When the voltage at the output of integrator U503 reaches the 7-V reference level of comparator U504, the comparator output goes high, quickly charging the squelch hang capacitor C502 fully. In turn, the output of timer U505 goes high. The resulting voltage, called SQ2, turns on a MOSFET muting buffer before the product detector, and a JFET muting switch in the receiver audio circuit; these are described below. The R502-C502 circuit provides the seven-second squelch hang time.

The squelch circuit is enabled by opening switch S2. This accomplishes several things. The voltage, SQ3, at the inverting input to timer U505 is switched from –3 V, for normal receiver operation, to +6 V for squelch functioning. This same SQ3 is also used with U206 in the main section to enable the panel SQUELCH LEVEL control. The squelch switch, S2, with U205, disables the panel IF GAIN control. Switch S2 also controls the squelch input switch U502 and the hang defeat switch U306, in the hang section. When the squelch is turned off, S2 discharges the squelch hang capacitor C502 and, using U506, resets the integrator. This elaborate squelch on/off switching is required for convenience in setting the SQUELCH LEVEL control because of the time hysteresis action of the integrating squelch circuit, as described in Note 2, and because of the hang action now incorporated.[3] The integrator capacitor voltage is monitored by the squelch meter, M2. The squelch threshold is about midscale on the meter. When transmitting SSB, this meter monitors the RF speech clipping level. No switching of meter function is required, nor is a summing op amp needed. For clipping level, the meter is driven similarly by an op amp in the transmitter section of the radio, which is disabled during receive. The driving circuit not in use merely presents a 15-kΩ load to the meter, which means nothing to a 100-Ω, 1-mA meter.

Associated Circuits

The MOSFET IF amplifiers controlled by this AGC system have no unusual features; the schematic of a typical 9-MHz stage is shown in Fig 12. Gain control is by means of gate 2, known as the "gain control gate." A typical curve of gain versus control gate voltage is shown in Fig 10, taken from the RCA 3N140 spec sheet. Notice the pronounced upper and lower knees. With the range of control voltage used, operation is in a fairly straight portion of the curve; this results in a nearly linear voltage-versus-dB relationship for easy S-meter calibration. The MOSFETs used here are type 3N140, but any small-signal RF-type dual-gate MOSFET may be used; they all have roughly the same characteristics at IF frequencies.

After the six gain-controlled stages, and before the product detector, a MOSFET buffer is used as a squelch gate, as shown in Fig 13. The squelch circuit produces a +15/–15 control voltage, SQ2; the voltage divider at the buffer reduces this to +4/–4 V, yielding full-gain/cut-off for gate 2 of the MOSFET. This buffer is also used for T/R muting using gate 1. With the resistive load in the drain circuit, this MOSFET circuit is convenient for unity-gain buffering and switching. The value of the drain resistor may be varied somewhat for small gain adjustments. Another squelch and T/R muting gate is in the audio section; it uses a JFET, as shown in Fig 14.

An AGC Test Device

Although a QRP transmitter can be used to generate the initial dits required for testing an AGC circuit, it was much more convenient to use a special pulse generator with a signal generator. A keyer producing a string of dits cannot be used. We need to monitor the AGC action on the *first* dit, then allow the AGC system to recover fully, and the receiver to resume maximum gain, before confronting the receiver with the next dit.

The pulse generator will produce spaced dits, with both the dit width and the spacing adjustable. It is used to select the proper values of R204-C204. The make/break timing for the pulse is 2 ms, soft enough so that any click heard, or seen on the scope, would be receiver-generated rather than the

actual signal. But too-soft timing here would make it *too easy* for the AGC system. The generator can be adjusted for pulses up to 100 ms, with spaces up to 10 s. I find that settings for 40-ms pulses (corresponding to dits at 30 wpm), spaced two seconds, work well.

The schematic is shown in Fig 15. The pulse generator is used to control an HP8640B signal generator. The PULSE input to the generator cannot be used because in this mode the generator produces very fast rise and fall times, merely triggered by the pulse input. The generator output does follow the level at the AM input, however; we use the AM-dc input. (This supports the idea that CW is really a form of AM.) The SIG GEN output of the pulse generator is configured to produce ±1 V at the 600-Ω AM-dc input to the HP generator, which has a control for further adjustment. The SCOPE output of the pulse generator is used to monitor the pulse width and space time. The two scope traces are then variously used to monitor the actual signal at points in the IF strip, the two AGC voltages and the receiver AF output. The pulse generator SCOPE output is used for triggering at the *end* of one pulse, using the delayed sweep to monitor the next complete pulse.

The pulse generator is powered by a ±15-V bench supply. There is no ground connection to the pulse generator; the ground reference is the ground connection at the bench supply.

The CW waveform shaping is obtained with the 100-kΩ, 0.02-μF timing circuit. The 2-ms timing produces a fairly hard CW keying waveform, but this is realistic for nearby signals heard in the DX bands. To distinguish AGC clicks from the natural sound of sharp CW, turn off the AGC and use the RF gain to hear the actual signal.

Acknowledgments

The idea for the hang AGC circuit was found in the Signal/One CX7 transceiver (1969). The AGC detector, first buffer, timing capacitors and discharge transistor (including the floor idea) are essentially as found in the CX7. The CX7 AGC system used 10 transistors and no op amps. The idea for a dual-attack AGC to eliminate pops, clicks, and overshoot, was found in the Drake 2-B receiver (1958).

Summary

Ham radio operation places special demands on a receiver. One of the most difficult requirements to meet is adequate AGC performance. Ironically, at times we really don't need any AGC for the S1 DX signals we want to hear; we need it to keep the domestic stations, whom we'd rather not hear at all, from cracking our skulls. This AGC system deals with the attack, hang and recovery problems, and eliminates pops, clicks and overshoot.

Notes

[1]The term *comparator* is ambiguous. Referring to devices, it means an op amp with an open collector output, such as the LM339. Referring to circuit function, however, the term may refer to such a comparator, or, as in this instance, an ordinary op amp used to compare levels.

[2]Mandelkern, Mark, "A Sensitive Integrating Squelch Circuit," *QST*, August 1988, pp 27-29.

[3]One design requirement was to provide switching of the squelch circuit with a single wire to the front panel. Wire harness overload was perhaps the toughest problem that arose in the three years of building this transceiver. This also explains the circuits used for IF GAIN, SQUELCH LEVEL and AGC HANG TIME. □□

Corrections for:

A High-Performance AGC System for Home-Brew Transceivers, QEX, October, 1995, pages 12-22.

Mark Mandelkern, 1999 December 21

1. Fig 5, lower right. The meter should be labeled "M2 - SQUELCH/CLIPPING". See also item 6 below.

2. Fig 5, upper left. Detector section should indicate Q101-Q103.

3. Fig 5, upper center. Main section should indicate Q201 thtough U203.

4. Fig 5, left. Hang section should indicate U301-U305.

5. Fig 5, right. M1 should be labeled "SIGNAL/ALC".

6. NOTE on the meter designators. In the later series on the transceiver, the M1-M2 meter labels were unfortunately reversed. Each meter is driven by 2 or more circuits. There are no relays or switching circuits; at most one meter driving circuit is active at any given time.

7. Fig 7, output of U202. The unlabeled terminal should be labeled: "Va - To S-Meter section".

8. Fig 7, output of U202, unlabeled resistor. 100k.

9. Fig 7, upper center. The trimpot labeled "Tx GAIN ADJUST" should be labeled "TX Gain Adjust". (Labels in all caps are reserved for front panel controls.)

10. Fig 7, lower left. U204 should have a dot at the output. This indicates an LM339 (see caption).

11. Fig 9. The meter should be labeled "M1 - SIGNAL/ALC".

12. Fig 9, left. The Va terminal could be annotated: From main section, Fig 7, second buffer, U202.

13. Fig 7, 7815. The IN and OUT terminals should be reversed. Note: The large 1000 mike capacitor is at the output of the regulator in order to supply a large transient current to Q201, to charge C201 and C202. This insures a fast AGC attack, and keeps this transient out of the rest of the circuit. The +18 line is well-regulated, so the input to the regulator needs only a small filter cap. This regulator in Fig 7 supplies only Q201. The remainder of the AGC subsection obtains +15 V from the main 7815 on the IF board; this ensures that transients from Q201 are isolated from the rest of the circuit.

14. Fig 11. The various terminals deserve some explanation.

SQ1. This is the Squelch switch S2. It connects to 2 points in Fig 11, to discharge the timing capacitor and to disable the timer, and to one point in Fig 7, to defeat the IF GAIN panel control. Indirectly, SQ1 also drives terminals SQ3 and SQ4.

SQ2. This is the output of the squelch circuit, driving the muting stages on the IF board.

SQ3. Connects to U206 in Fig 7 to enable the SQUELCH LEVEL control.

SQ4. In Fig 11 this line resets the integrator. In Fig 8 it defeats the AGC Hang circuit when in Squelch mode.

The purpose of some of the squelch switching lines is to fully discharge all the squelch circuits when the Squelch is switched off. This facilitates adjustment of the squelch level panel control. Otherwise the operator would have to wait until after the 7 second squelch hang time (see p 21) before re-adjusting the level.